High-Accuracy All-Digital Resolver-to-Digital Conversion

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***Abstract*—In this paper, a high-accuracy all-digital resolver-to-digital (R/D) converter is presented. The two basic components of a conventional tracking R/D converter, the phase detector and the loop filter, are software implemented by frequency-shifting techniques and a decoupled double synchronous reference frame-based phase-locked loop (DSRF-PLL). This PLL allows the simultaneous extraction of the angular position and speed of the rotatory resolver, even in the presence of gain and phase errors in the resolver. In order to increase accuracy and to minimize the time lag of the whole system, oversampling methods and down-sampling finite-impulse response digital filters are introduced. Finally, DSP implementation issues, like the use of techniques to synchronize the resolver output signals with the excitation one, are discussed. Using these combined techniques and a standard DSP with a 12-bit analog-to-digital converter, resolutions of up to 14 bits can be achieved with a computation cost of about 13% of the total (100 MIPs). The paper presents the main techniques, simulation, and experimental results.**

***Index Terms*—Digital filters, DSPs, oversampling, phase-locked loops (PLLs), resolver, resolver-to-digital (R/D), variable speed drives.**

I. Introduction

ADJUSTABLE SPEED DRIVES (ASDs) have become increasingly more accurate and precise and have better transient responses. One of the important areas of research interest is velocity and position control loops. While many investigations are trying to eliminate the need for position or velocity sensors (usually encoders or resolvers) and developing the sensorless ASD ([1] and [2]), many industrial applications still rely on the feedback of accurate angular position sensing systems, namely, position control loops within numerical machine tools, robot arms, and others [3]–[5]. The main purpose of the sensorless ASD is to reduce the total equipment cost. This paper proposes a different approach to achieve the same goal, namely, to implement the external resolver-to-digital (R/D) converter IC as an all-digital R/D conversion.

Several methods for R/D conversion, e.g., [6]–[8], exist in the literature. Some focusing on increasing measurement accuracy of the R/D conversion, some on simultaneously obtaining speed information from R/D conversion, and yet some others on cost-effective techniques.

In [9], Bunte and Beineke introduce methods for eliminating systematic resolver errors, such as gain, phase, offset, and harmonic errors. Among these, only gain and phase errors need to be considered, as offset errors are corrected by the frequency-shifting technique [10] combined with the oversampling method [11], as described in Section II, whereas harmonic errors are typically negligible, with total harmonic distortion being less than 0.01% [12]. This paper, in Section IV, presents a methodology to suppress gain and phase errors based on the double synchronous reference frame-based phase-locked loop (DSRF-PLL) [13].

In [14] and [15], Bellini *et al.* present a steady-state linear Kalman filter-based PLL to obtain velocity information by reducing noise from the derivative operation. Despite using a similar technique to the one described here, the Kalman filter has the expected angular acceleration of the shaft, which is not always available, as input. Moreover, the Kalman filter has the disadvantage that the gain vector for correcting the predicted state, which plays an important role in the dynamic characteristics of the speed control loop, includes a trial-and-error selection procedure, making this technique difficult to implement.

In [16], Sarma *et al.* propose a software-based R/D conversion using a DSP as a simple cost-effective R/D converter. The method is based on not fulfilling the Shanon sampling theorem while benefiting from aliasing to demodulate the sine and cosine resolver signals. Unfortunately, it is rather inaccurate [resolution limited to that of the DSP analog-to-digital converter (ADC)] and lags velocity extraction [17].

Finally, in [18], Ben-Brahim *et al.* present a resolver angle estimation method based on the comparison of the amplitude of the resolver signals, the excitation signal and another signal shifted by $\pi/2$. The technique is easy to implement as it requires neither a processor nor a lookup table and is robust to amplitude excitation changes. However, it does not provide adequate resolution and accuracy for high-performance position control loops, lags velocity extraction, and does not correct resolver errors.

In [17], the authors propose an all-digital R/D conversion which presents, at the same time, a high degree of accuracy [19] and a simple and cost-effective solution. To increase the accuracy of R/D conversion measurements and the resolution of the whole system, this conversion (based on the frequency shifting technique) is combined with an oversampling method.

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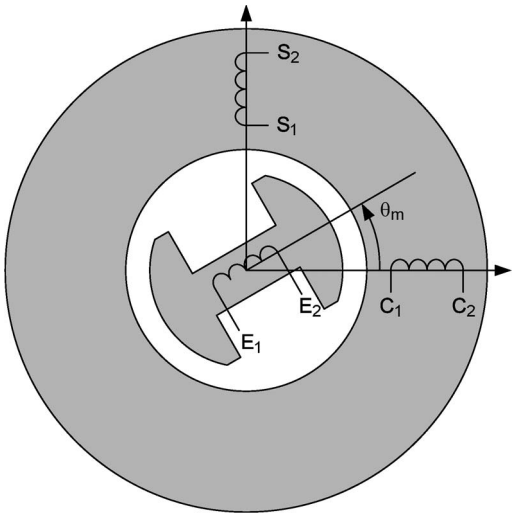

Fig. 1. Schematic of a resolver. E_1–E_2 represent the excitation rotor coil while S_1–S_2 and C_1–C_2 are the sine and cosine stator coils, respectively.

The mechanical angle and speed are obtained by using an synchronous rotating reference frame-based (SRF)-PLL, with an increasing filtering effect, and simultaneously compensating for the delay intrinsic to the digital filter of the downsampling.

In this paper, we outline the most relevant results in [17]. One of the problems stated in the latter paper is associated with the synchronization of the sine- and cosine-modulated resolver signals with the reference generated by the DSP. Section III describes a resynchronization algorithm to deal with delays in the filtering system and the resolver. Other problems are related to resolver gain and phase errors, now here addressed with a DSRF-PLL instead of the simple SRF-PLL used in [17]. As pointed out in Section IV, this PLL extracts resolver angular position and speed simultaneously even in the presence of resolver gain and phase errors. Additionally, new experimental results obtained with a TMS320F2808 DSP from Texas Instruments Incorporated are presented, with higher ADC resolutions (12 bits) and an increase in the oversampling factor, due to the superior mathematical power of these DSPs.

This paper is organized as follows. In Section II, an overview of the whole system is given. Section III describes the dephasing algorithm tracking. The methodology to suppress systematic resolver errors is described in Section IV, while experimental results are provided in Section V. Finally, Section VI draws conclusions.

II. Overview of the Whole System

Fig. 1 shows the schematic of a two-pole resolver. The excitation coil (E_1–E_2) resides in the rotor and is usually fed by means of brushes or magnetic coupling from the stator, with a sinusoidal voltage (1) of frequency $f_e = \omega_e/2\pi$ in the range between 4 and 10 kHz. S_1–S_2 and C_1–C_2 are two quadrature stator coils, usually known as the sine and the cosine coils, respectively.

$$V_E = V_{0e}\cos(\omega_e t). \tag{1}$$

Equations (2) and (3) show the voltages induced in both stator coils when the excitation signal is applied to the rotor coil ([20] and [21]). These two signals are the excitation signals multiplied (modulated) by the sine and cosine of the mechanical angle (θ_m) as follows:

$$V_S = V_0\left[\cos(\omega_e t)\sin(\theta_m) + \frac{\omega_m}{\omega_e}\sin(\omega_e t)\cos(\theta_m)\right] \tag{2}$$

$$V_C = V_0\left[\cos(\omega_e t)\cos(\theta_m) - \frac{\omega_m}{\omega_e}\sin(\omega_e t)\sin(\theta_m)\right] \tag{3}$$

where $V_0 = kV_{0e}$ is a constant that depends on the transformer ratio of the resolver (k) and the excitation level (V_{0e}); and θ_m is the position to be decoded and in general is a function of time $\theta_m = \int_0^t \omega_m d\tau + \theta_m(0)$, where ω_m is the mechanical speed of the shaft to be sensed. Normally, $f_m = \omega_m/2\pi$ is below 200 Hz, which corresponds to 12 000 r/min in a two-pole resolver. Thus, the term affected by ω_m can be ignored when dealing with low speeds (ω_m is much smaller than ω_e), thereby obtaining the following:

$$V_S = V_0\cos(\omega_e t)\sin(\theta_m) \tag{4}$$

$$V_C = V_0\cos(\omega_e t)\cos(\theta_m). \tag{5}$$

Tracking R/D conversion consists of extracting the shaft position from both generated signals (V_S and V_C). A traditional way of obtaining the mechanical angle from signals V_S and V_C is the so-called undersampling technique [16], [17]. This method takes one pair of samples at every period of the excitation frequency; in doing so, the Shannon sampling theorem is not fulfilled, leading to the demodulation of both signals by aliasing. With these two samples, it is easy to obtain the mechanical angle θ_m with a four-quadrant inverse tangent function [22]. However, despite being feasible and nonintensive, this method has some drawbacks [17] as follows:

- Samples of the sine and cosine signals have to be taken at the maximum of the sinusoid to achieve the maximum possible accuracy. Variable delays make it difficult to keep the synchronization of the sampling instant.
- The calculation of the mechanical angle depends on only one sample of the sine and cosine signals, which can lead to inaccuracies due to electromagnetic compatibility problems.

In order to overcome the drawbacks of the undersampling method and to obtain the mechanical angle more precisely, a more sophisticated algorithm with oversampling and frequency shifting is proposed. Higher resolution in R/D position sensing can be achieved by the oversampling technique [23]. This method is based on the fact that the analog signal is sampled at a much higher frequency than that at which the signal is needed. The sampled signal is then digitally filtered to obtain an averaged value and downsampled again using decimation (Fig. 4). Equations (4) and (5) represent the signals in the sine and cosine coils, respectively, which can be read as amplitude-modulated sinusoids and be rewritten as follows:

$$V_S = \frac{V_0}{2}\left[\sin(\omega_e t + \theta_m) - \sin(\omega_e t - \theta_m)\right] \tag{6}$$

$$V_C = \frac{V_0}{2}\left[\cos((\omega_e t + \theta_m) + \cos((\omega_e t - \theta_m)\right]. \tag{7}$$

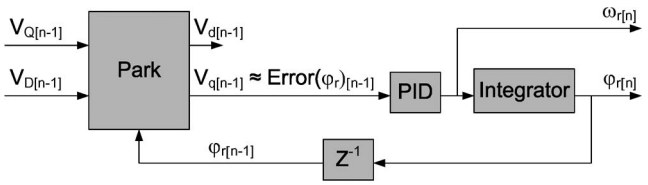

Fig. 2. SRF-PLL. This SRF-PLL has extra filtering obtains the mechanical speed directly and compensates for the delays.

In the frequency domain, the spectrum power of these signals, once convoluted with the excitation one, is divided into two different regions. The first is centered in the low frequencies (a region centered in zero and a width of ω_m) while the second moves to the high frequencies (a region centered in ω_e and with the same width as previous region).

The convolution is done by multiplying (4) and (5) by the excitation signal $\cos(\omega_e t)$

$$V_{S2} = \cos(\omega_e t) V_S = V_0 \cos^2(\omega_e t)\sin(\theta_m) \tag{8}$$

$$V_{C2} = \cos(\omega_e t) V_C = V_0 \cos^2(\omega_e t)\cos(\theta_m). \tag{9}$$

Once reduced, these equations become

$$V_{S2} = \frac{V_0}{2}\sin(\theta_m) + \frac{V_0}{2}\left[\frac{\sin(2\omega_e t + \theta_m) - \sin(2\omega_e t - \theta_m)}{2}\right] \tag{10}$$

$$V_{C2} = \frac{V_0}{2}\cos(\theta_m) + \frac{V_0}{2}\left[\frac{\cos(2\omega_e t + \theta_m) - \cos(2\omega_e t - \theta_m)}{2}\right]. \tag{11}$$

As the mechanical frequency (f_m) is much lower than the electrical frequency (f_e), both signals can be low-pass filtered and the low-frequency components of the latter can be isolated [this filter is usually combined with the decimation finite-impulse response (FIR) filter of the oversampling process]

$$V_{S3} = \frac{V_0}{2}\sin(\theta_m) \tag{12}$$

$$V_{C3} = \frac{V_0}{2}\cos(\theta_m). \tag{13}$$

Next, instead of using the four-quadrant inverse tangent function, an SRF-PLL is applied (Fig. 2) to obtain the mechanical angle θ_m [24]. This approach has several advantages such as the following.

- The integral part of the PID controller provides an additional filtering effect.
- The mechanical speed is obtained directly.
- In stationary state, the delay created by a software FIR filter applied to the input signals can be corrected. This is the case, for example, when an oversampling technique is used to increase angular resolution.

The two inputs to the SRF-PLL are V_{S3} and V_{C3}, which will be called V_Q and V_D, respectively, for standard convention. They represent the two components of a vector $\vec{V}$ with an amplitude of $V_0/2$ and an angle θ_m in a stator fixed reference frame. This vector can be expressed in a new reference frame by rotating it at an angle of θ_r with respect to the fixed one using the Park transformation (14). In this new rotating reference frame, the two components of the vector $\vec{V}$ are V_d and V_q (Fig. 3).

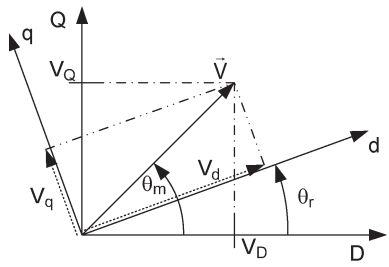

Fig. 3. SRF. D and Q are two orthogonal stationary axes while d and q are two orthogonal rotating axes. $\vec{V}$ is the vector with V_D and V_Q in the first reference and V_d and V_q in the rotating reference.

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \cos\theta_r & \sin\theta_r \\ -\sin\theta_r & \cos\theta_r \end{bmatrix} \begin{bmatrix} V_D \\ V_Q \end{bmatrix}. \tag{14}$$

When θ_r tends to equal θ_m, the V_q component tends to zero, somehow representing the shift error between the two angles [25]

$$V_q = \frac{V_0}{2}\sin(\theta_m - \theta_r) \overset{\theta_r \to \theta_m}{\approx} \frac{V_0}{2}(\theta_m - \theta_r). \tag{15}$$

A second-order closed-loop controller (formed by a PID plus a null pole integrator) keeps the V_q component near null by locking to the input angle [26]. Minimization of the V_q component results in two possible positions, both of which are dephased 180°, but only one is stable. The output of the PID gives the estimated speed, and after its integration, the estimated angle. The latter is used to refeed the system at the rotation angle input of the Park transformation. It must be pointed out that the settling time of the PID imposes maximum possible mechanical acceleration.

III. Dephasing Algorithm Tracking

In an all-digital R/D conversion, the DSP must generate the excitation signal while at the same time demodulating the two encoded incoming signals. The usual way of generating the excitation signal is through a pulse width modulation (PWM) output, followed by an analog filter (Fig. 4). This filter, combined with drifts in the resistance of the resolver coils due to temperature variations, causes a detuning angle to appear between the excitation signals generated internally by the DSP and the real excitations seen by the resolver transformer as follows:

$$V'_S = V_0 \cos(\omega_e t - \phi)\sin(\theta_m) \tag{16}$$

$$V'_C = V_0 \cos(\omega_e t - \phi)\cos(\theta_m) \tag{17}$$

where ϕ is the phase shift between the input and output excitation signals.

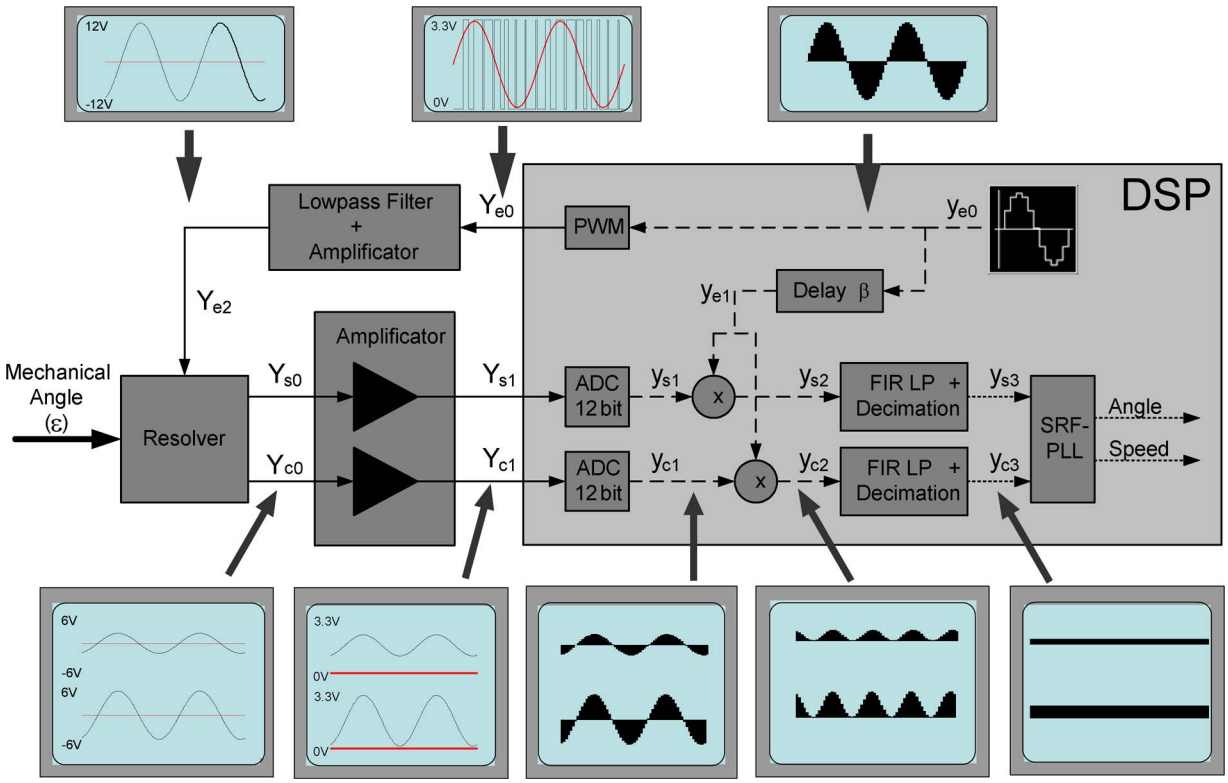

Fig. 4. Functioning diagram of the complete system, comprising the excitation signal generation, (in the figure, y_{e0} is the internal DSP value, y_{e1} is the PWM voltage at a commutating frequency of 288 kHz, and finally, y_{e2} is the same signal once filtered); the delayed excitation signal y_{e1}; the sine and cosine signals from the resolver (Y_{s0} and Y_{c0}), before and after their amplification (Y_{s1} and Y_{c1}); (y_{s1} and y_{c1}) are the resolver signals once discretized, and before being convoluted with the dalayed excitation signal y_{e1}; afterward these signals are low-pass filtered and decimated (y_{s3} and y_{c3}) in the same FIR filter which combine the two functions; and finally, these signals enter the SRF-PLL in order to extract the angle and speed of the resolver. Solid lines represent analog signals, dashed lines represent signals at 288 kHz, and pointed lines represent signals at 4.5 kHz.

Proceeding as in Section II, once demodulated, the resolver signals become [17]

$$V'_{S3} = \frac{V_0}{2}\sin(\theta_m)\cos(\phi) \tag{18}$$

$$V'_{C3} = \frac{V_0}{2}\cos(\theta_m)\cos(\phi). \tag{19}$$

This reduction in the filtered signal can decrease system accuracy if $\cos(\phi)$ reaches critically low values. In the worst scenario, the delay angle may be 90°; and therefore, $\cos(\phi) = 0$, in which case the whole system would not function at all.

To avoid this reduction of accuracy, an equalization method consisting in dephasing the demodulation signal to maximize incoming filtered signals is proposed. The demodulation signal is dephased by an angle β, as shown in Fig. 4

$$\begin{aligned} V''_{S2} &= \cos(\omega_e t - \beta)V'_S \\ &= V_0\cos(\omega_e t - \beta)\cos(\omega_e t - \phi)\sin(\theta_m) \end{aligned} \tag{20}$$

$$\begin{aligned} V''_{C2} &= \cos(\omega_e t - \beta)V'_C \\ &= V_0\cos(\omega_e t - \beta)\cos(\omega_e t - \phi)\cos(\theta_m). \end{aligned} \tag{21}$$

As described in Section II, once manipulated and filtered, the signals become

$$V''_{S3} = \frac{V_0}{2}\sin(\theta_m)\cos(\phi - \beta) \tag{22}$$

$$V''_{C3} = \frac{V_0}{2}\cos(\theta_m)\cos(\phi - \beta). \tag{23}$$

The dephasing algorithm consists of controlling β until $\beta = \phi$. The closer β gets to ϕ, the higher the amplitude of V''_{S3} and V''_{C3}. A first implementation could be the simultaneous maximization of V''_{S3} and V''_{C3} by the modification of β. Nevertheless, since both signals are a sinusoidal function of time, it is not straightforward to determine their maximum. A more appropriate function is the sum of squares of V''_{S3} and V''_{C3}, which remains constant over time

$$\begin{aligned} V''^2_{S3} + V''^2_{C3} &= \frac{V_0^2}{4}\cos^2(\phi - \beta) \\ &\overset{\phi\to\beta}{\approx} \frac{V_0^2}{4}. \end{aligned} \tag{24}$$

As a figure of merit of this condition, the V_d component of the Park transformation in the previous section could be taken

$$\begin{aligned} V_d &= \frac{V_0}{2}\cos(\theta_m - \theta_r) \\ &\overset{\theta_r\to\theta_m}{\approx} \frac{V_0}{2} = \sqrt{V''^2_{S3} + V''^2_{C3}}. \end{aligned} \tag{25}$$

This would simplify the operations (which have to be performed anyway). It is worth noting that this algorithm is much easier to implement in a DSP than the variable sampling instant solution presented in [17]. It is only necessary to calculate the cosine signal dephased with respect to the excitation signal, which is already generated in the DSP (Fig. 4). Moreover, this

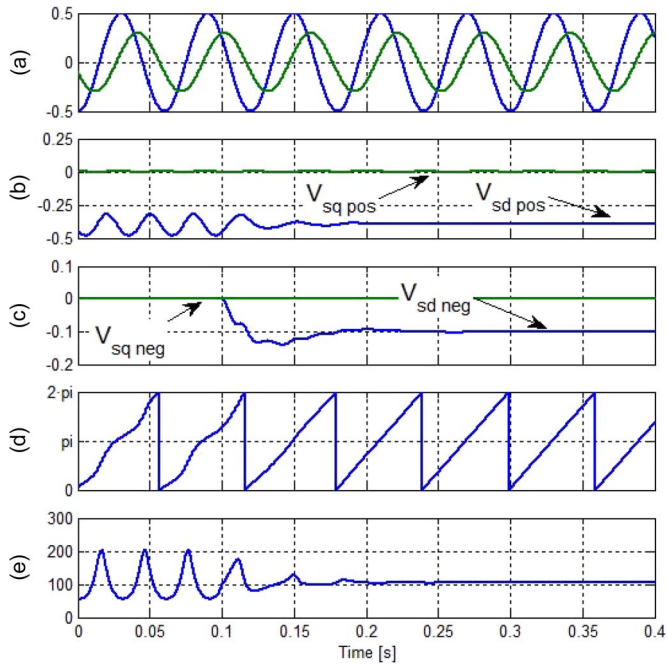

Fig. 5. Simulation results for the resolver signals with systematic errors (gain and phase errors). At the initial time, the DSRF-PLL functions as an SRF-PLL, and at time = 100 ms, it starts functioning as a DSRF-PLL. (a) Sine and cosine resolver signals (cosine signal is 40% lower than sine one and dephased 70° instead of 90° as it should be). (b) Direct and quadrature components of the positive sequence of the DSRF-PLL. (c) Direct and quadrature components of the negative sequence of the DSRF-PLL. (d) Resolver angle estimation with the DSRF-PLL. (e) Speed estimation.

dephased angle β can be dynamically adapted to take into account variable delays that could occur in electrical components due to variations in temperature and age.

IV. Systematic Resolver Errors Suppression

Resolvers are not ideal electrical machines [9], [27]. When studied in detail, sine and cosine signals must be considered as not perfectly sinusoidal; as a result, errors such as the following may occur:

- Offset errors, that is, there is an offset in one or both signals.
- Gain errors, that is, there exist differences between the amplitudes of the sine and cosine signals.
- Phase errors, that is, the sine and cosine signals are not perfectly in quadrature.

Offset errors are eliminated by the frequency-shifting technique because dc signal components are brought to the high-frequency side of the spectrum where they are eliminated by a low-pass filter. If not properly corrected, gain and phase errors result in position and speed errors (as shown in Fig. 5). In this section, a way of suppressing the former errors is proposed.

In a first approximation, let us suppose that the resolver has only a gain error which, without loss of generality, can be assumed to be all concentrated in the sine signal. The sine and cosine signals are then rewritten as

$$V_S = V_1 \alpha \sin(\theta_m) \tag{26}$$
$$V_C = V_1 \cos(\theta_m) \tag{27}$$

where $V_1 = V_0/2$.

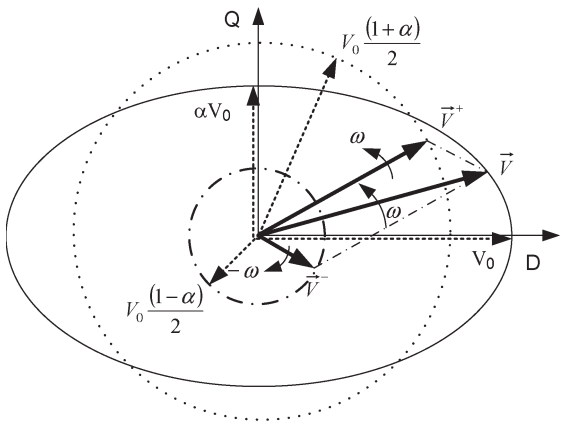

Fig. 6. Decomposition of the unbalanced resolver signals $\vec{V}$ (the cosine signal has a larger amplitude than the sine signal) into two balanced vectors (one a positive rotating vector, $\vec{V}^+$, and a negative rotating one, $\vec{V}^-$).

Once plotted in an orthogonal plane (the cosine signal in the horizontal axis and the sine signal in the vertical one), the signals represent an ellipse of a width of V_1 and a height of $V_1\alpha$ (Fig. 6). If α is equal to one, that is, there is no gain error, and the ellipse becomes a perfect circle.

Another way of interpreting these two signals is to look at them as a rotating vector of nonconstant amplitude. This vector can be decomposed into the sum of a positive rotating vector ($\vec{V}^+ = [V_D^+, V_Q^+]^T$) plus a negative rotating one ($\vec{V}^- = [V_D^-, V_Q^-]^T$)

$$\begin{bmatrix} V_1 \cos(\theta_m) \\ V_1 \alpha \sin(\theta_m) \end{bmatrix} = \left[T_{dq}^-\right] \vec{V}^+ + \left[T_{dq}^+\right] \vec{V}^- \tag{28}$$

where $\vec{V}^+ = [V_1((1+\alpha)/2), 0]^T$ and $\vec{V}^- = [V_1((1-\alpha)/2), 0]^T$ are the components of the positive and negative rotating vectors, respectively (Fig. 6); and $[T_{dq}^+]$ and $[T_{dq}^-]$ are the rotating matrix and its inverse

$$\left[T_{dq}^+\right] = \begin{bmatrix} cos\theta_m & \sin\theta_m \\ -\sin\theta_m & \cos\theta_m \end{bmatrix} \tag{29}$$

$$\left[T_{dq}^-\right] = \begin{bmatrix} cos\theta_m & -\sin(\theta_m) \\ \sin\theta_m & \cos\theta_m \end{bmatrix}. \tag{30}$$

If these unbalanced resolver signals, which represent an ellipse in the orthogonal plane (the stationary reference frame given by the two orthogonal axes D and Q), enter the SRF-PLL in Fig. 3, the variable amplitude of the ellipse would be interpreted as a vector whose rotating speed accelerates and decelerates, as shown by the plot of the angle as a function of time in the first part in Fig. 5.

A DSRF-PLL [13] is similar to the SRF-PLL in Section II. However, by using a positive rotating reference frame in combination with a negative rotating one (Fig. 7), the DSRF-PLL cleanly extracts and separates the positive- and negative-sequence components of the input vector. It is worth mentioning that the sine and cosine signal amplitudes are not important. What really matters is that both signals have the same amplitude.

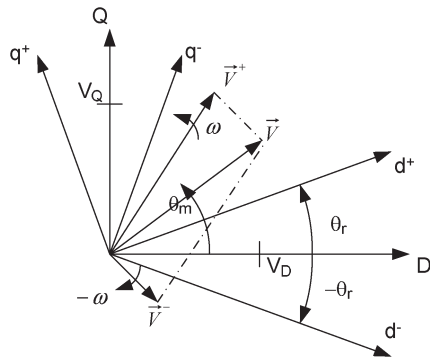

Fig. 7. DSRF. $\vec{V}$ is the vector the components of which are the sine and cosine resolver signals. $d^+ - q^+$ and $d^- - q^-$ are the two reference frames rotating at ω and $-\omega$, respectively. V^+ and V^- are the positive and the negative sequences, respectively, into which vector $\vec{V}$ can be decomposed.

Finally, in the presence of gain and phase errors, we can decompose the rotating vector into two other vectors, both of which are unbalanced but with no phase error

$$\begin{bmatrix} V_1\cos(\theta_m) \\ V_1\alpha\sin(\theta_m+\beta) \end{bmatrix} = \begin{bmatrix} V_1\cos(\theta_m) \\ V_1\alpha\cos(\beta)\sin(\theta_m) \end{bmatrix} + \begin{bmatrix} 0 \\ V_1\alpha\sin(\beta)\cos(\theta_m) \end{bmatrix}. \quad (31)$$

In some sense, we have converted a problem of phase error into a problem of gain error. If we now decompose these two vectors in its positive and negative sequences, as has been presented before for the gain error case, we obtain

$$\begin{bmatrix} V_1\cos(\theta_m) \\ V_1\alpha\sin(\theta_m+\beta) \end{bmatrix} = \left[T_{dq}^-\right]\vec{V}_p + \left[T_{dq}^+\right]\vec{V}_n \quad (32)$$

where now the different parameters take next values

$$\vec{V}_p = V_1\begin{bmatrix} \frac{(1+\alpha\cos(\beta))}{2} \\ \frac{\alpha\sin(\beta)}{2} \end{bmatrix} \quad (33)$$

$$\vec{V}_n = V_1\begin{bmatrix} \frac{(1-\alpha\cos(\beta))}{2} \\ \frac{\alpha\sin(\beta)}{2} \end{bmatrix}. \quad (34)$$

That is, in the most general case, when the sine and cosine resolver signals have different amplitudes and are dephased an angle other than 90 degrees, the DSRF-PLL extracts their positive component and the real angle, and estimate the speed, as can be seen in the second part in Fig. 5.

V. Simulation, Experimental Implementation, and Results

To evaluate the performance of the whole system, several simulations were carried out. Fig. 5 shows the results of the simulation of the whole system. In this simulation, both amplitude and quadrature errors were introduced. The amplitude mismatch between the sine and cosine signals was 40%, and the dephasing error was 20° with respect to the quadrature. These are high errors, much more than one could expect to find in a commercial resolver. This has been done in this way

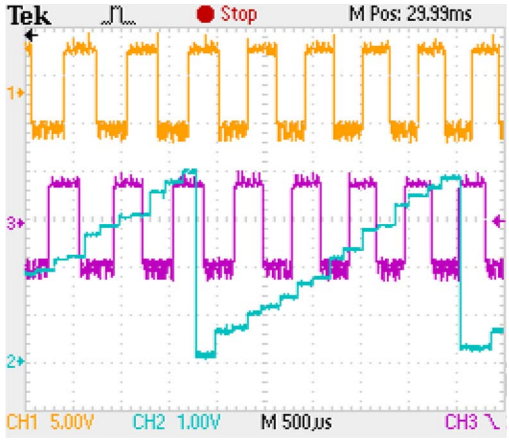

Fig. 8. Experimental results for the two quadrature encoder pulses and the resolver calculated angle shown by the DAC. Channels 1 and 3 are the two quadrature encoder signals, while channel 3 is the measured resolver angle, with a resolution of between three to four times that of the encoder.

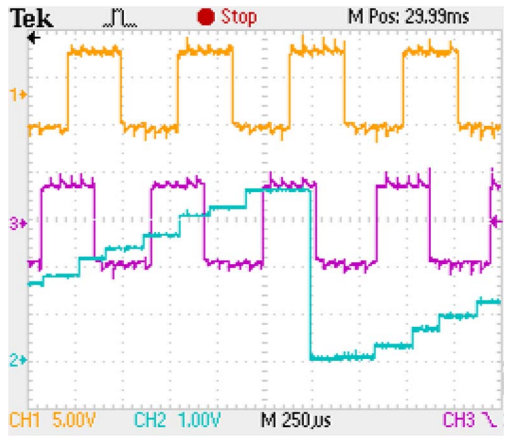

Fig. 9. Zoom of the oscilloscope in Fig. 8, for better appreciation of the resolution of the calculated angle. Considering that the encoder delivers 2048 pulses per revolution, which represents 11 bits, and that the measured resolver angle presents a resolution of between three to four times that of the encoder. From this scope, one can conclude that the resolution of the measured angle is between 13 to 14 bits.

in order to emphasize the proposed algorithm ability to deal with such errors, in contrast to the traditional one, which exhibits a pulsating speed estimation in these situations. Although implementation of the DSRF-PLL compared to the SRF-PLL represents nearly a 40% increment in the computational cost, it represents a merely 12% for the total algorithm: PLL, dephasing algorithm tracking, oversampling, and filter downsampling included. In the simulation, during the first 100 ms, the system was operated without the DSRF-PLL presented in Section IV. As a consequence, we find an error in the position and speed estimation. At time $t = 100$ ms, the DSRF-PLL was turned on, and when the transient was completed (nearly 100 ms later), both the position and speed were accurately estimated.

At the same time, an experimental setup was built and implemented with a Texas Instruments Incoporated DSP (TMS320F2808) to measure the resolution of the system. This 32-bit DSP is particularly designed for motor control and features, along with other dedicated peripherals, eight ADCs

with 12-bit resolution. The control board includes a digital-to-analog converter (DAC) of four channels, which are used to output DSP's variable values in real time. Besides the control board, the experimental setup included a brushless dc motor with a two-pole resolver and a quadrature encoder of 2048 pulses per revolution on the same axis.

The nominal excitation frequency of the resolver is 4.5 kHz, which is digitally generated with the PWM module of the DSP at an output frequency of 144 kHz. As mentioned in Section II, the sine and cosine signals of the resolver are oversampled with the aim of incrementing the whole system resolution. These signals are sampled at a frequency of 288 kHz and low-filtered and convoluted with the excitation signal meanwhile an FIR filter of 65 taps and cutoff frequency of 1 kHz. That represents an ovesampling factor of $k = 32$, since the Nyquist frequency is $2 \cdot 4.5$ kHz $= 9$ kHz. With this oversampling factor, the overall signal-to-noise ratio (SNR) is incremented SNR $= 10 \log_{10}(k)$ by 15 dB. For an ideal ADC, its SNR increases by 6.02 dB with each extra bit. In addition, when the input is a full-scale sine wave (that is, the ADC system is designed such that it has the same minimum and maximum values as the input signal) which is nearly the case in the resolver system, then the increment in the SNR is augmented by 1.76 dB. Thus, with the aforementioned oversampling, the resolution of the ADC (effective number of bits, ENOB) is theoretically increased by ENOB $= (\text{SNR} - 1.76)/6.02 = 2.2$ bits.

The whole system has been implemented in a 32-bit DSP, with a computation cost of about 13% of the total (100 MIPs). Figs. 8 and 9 show the quadrature encoder pulses and the calculated resolver angle shown by the DAC. In these figures, one can distinguish between three and four values of the calculated angle for every encoder pulse, that is, a resolution between three and four times higher than that of the encoder, which is of 11 bits. Therefore, the resolution of the calculated resolver angle is approximately of 13 to 14 bits, in agreement with the theoretical calculations.

VI. Conclusion

The high-accuracy all-digital R/D conversion has been implemented satisfactorily. The two main objectives of an angular transducer were reached, i.e., high-resolution measurements of the angle by extraction techniques and high immunity to systematic resolver errors, which can be corrected by the DSRF-PLL, at the same time of extracting the resolver speed. All of these have been achieved due to the DSPs techniques used in the R/D conversion; from the phase detector to the loop filter, all the stages of this conversion have been realized in software.

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