INVITED PAPER

The Evolution to Modern Phased Array Architectures

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ABSTRACT | Phased array technology has been evolving steadily with advances in solid-state microwave integrated circuits, analysis and design tools, and reliable fabrication practices. With significant government investments, the technologies have matured to a point where phased arrays are widely used in military systems. Next-generation phased arrays will employ high levels of digitization, which enables a wide range of improvements in capability and performance. Digital arrays leverage the rapid commercial evolution of digital processor technology. The cost of phased arrays can be minimized by utilizing high-volume commercial microwave manufacturing and packaging techniques. Dramatic cost reductions are achieved by employing a tile array architecture, which greatly reduces the number of printed circuit boards and connectors in the array.

KEYWORDS | Antenna array feeds; antenna arrays; digital beamforming; overlapped subarray; phased array radar; phased arrays; radar antennas; tile array

I. INTRODUCTION

Phased array technology has been evolving steadily since it was first conceived in the early 1900s [1]. Early antenna arrays had fixed beam-pointing and utilized mechanical rotation to steer the beams. It was not until the mid-1940s that the technology became available to steer a beam by mechanically controlling the phase shift at each element [2].

As shown by the timeline plot in Fig. 1, phased arrays have undergone a steady evolution over the past 55 years. Three general categories of phased arrays can be described as passive, active, and digital. A passive array is one in which the array is fed by a centralized high-power transmit amplifier, with a low-loss power-combining network and a phase shifter at every element. An active array is one where the transmit power amplifiers, low-noise amplifiers, and phase shifters are distributed throughout the array at the element level. A digital array is one where the radio frequency (RF) signals are converted to digital signals at the subarray or element level, with the beamforming being performed by a digital signal processor.

The development of electronic steering in phased arrays has its origin in the ballistic missile defense requirement of scanning large volumes of space for reentry bodies and tracking multiple objects for battle management. Rapid mechanical scanning of large high-power radar dishes over wide-angle sectors is not a feasible option. In 1958, the Advanced Research Projects Agency (ARPA) began a technology development program called Electronically Steered Array Radar (ESAR). This program demonstrated the first two-dimensional, electronically steered, computer-controlled phased array radar. The program also included research and development in reliable high-power transmitter tubes and low-cost mixers and phase shifters.

In 1965, ARPA sponsored the development of the Hard Point Demonstration Radar (HAPDAR) as part of Project Defender [3]. HAPDAR was an L-band space-fed passive lens array with low-loss ferrite phase shifters. The AN/FPS-85 radar was developed between 1965–1969 by Bendix and deployed to Eglin Air Force Base (AFB) [4]. The AN/FPS-85 was an active phased array with high-power tube amplifiers at every element, operating at UHF-band. Another radar, the COBRA DANE, was developed by Raytheon and installed in 1977 on the island of Shemya in Alaska. COBRA DANE operates at L-band, and initially

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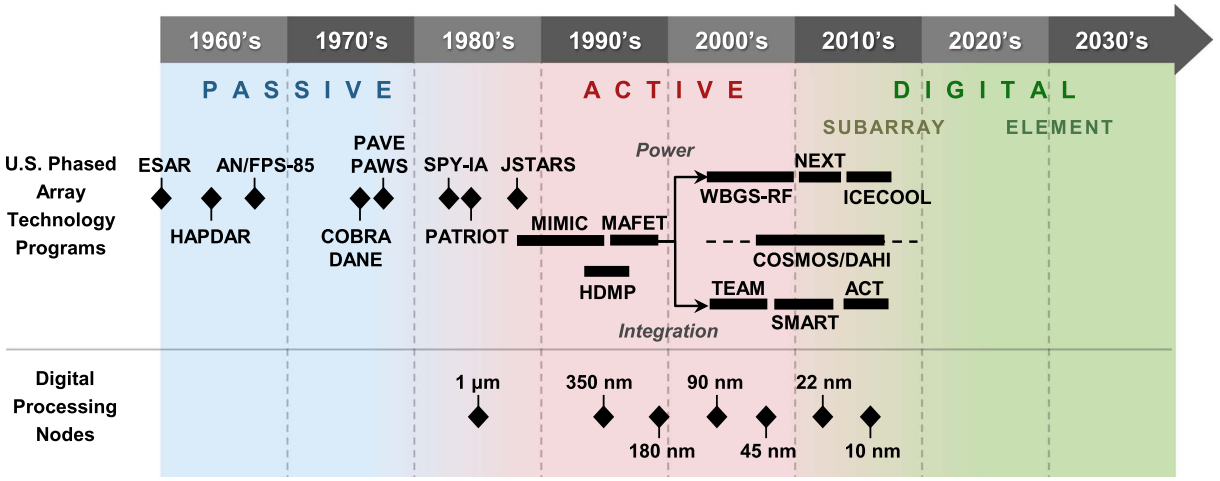

Fig. 1. *U.S. phased array technology development programs and digital processing nodes timeline.*

utilized vacuum tube transmit amplifiers feeding subarrays of elements. The PAVE PAWS radar was the first solid-state phased array radar, built by Raytheon and deployed in 1980 to Beale AFB and Otis AFB.

The phased array technology developed in the 1960s and 1970s for use in large missile warning and space surveillance radars was heavily leveraged in the development of large-scale production radars in the 1980s, including the S-band SPY-1A radar for the U.S. Navy, the C-band Patriot radar for the U.S. Army, and the X-band Joint Surveillance Target Attack Radar System (J-STARS) for the U.S. Air Force.

The Defense Advanced Research Projects Agency (DARPA) Microwave and Millimeter Wave Monolithic Integrated Circuits (MIMIC) program [5], which began in 1988 and ran through 1995, established robust, controllable manufacturing processes for gallium arsenide (GaAs) integrated circuit chips, multichip ceramic packages, accurate computer-aided device and circuit modeling tools, automated on-wafer testing techniques, and advanced fabrication methods. The DARPA High Density Microwave Packaging (HDMP) program [6], which ran from 1993 to 1996, focused on high-density packaging techniques for next-generation aircraft and space-based phased array radars, where thin conformal arrays are required. The DARPA Microwave and Analog Front End Technology (MAFET) program [7], which started in 1995 and ended in 1999, developed design tools, methodology, and models to support virtual prototyping of microwave and millimeter-wave multichip assembly modules. The goal of the MAFET effort was to replace the design-build-test methodology with a simulation-based methodology to achieve a significant reduction in design cycle time. These three programs were largely responsible for enabling the insertion of active phased arrays into fielded military systems starting in the 1990s.

As requirements for higher transmit power emerged in the late 1990s, it became clear that new technologies were needed to achieve higher power levels and operate at higher frequencies. At that point, two development paths were initiated—one to increase the output power and operating frequencies of solid-state amplifiers in arrays, and the other to increase the levels of integration in mixed-signal integrated circuits. The DARPA Wide Band Gap Semiconductor for RF Applications (WBGS-RF) program [8], which ran from 2002 through 2008, made a sustained investment in advancing the state of the art of Gallium Nitride on Silicon Carbide (GaN-on-SiC). GaN-on-SiC-based transistors enable high power-added efficiency (PAE) power amplifiers that have significantly higher output power and power density than is presently available from amplifiers based upon other materials such as GaAs or Indium Phosphide (InP). The DARPA Nitride Electronic Next Generation Technology (NEXT) program [9], which ran from 2010 through 2013, focused on enabling high-frequency (500 GHz) operation of GaN with high yield, uniformity, and reliability.

The DARPA WBGS-RF and NEXT programs were aimed at developing compound semiconductor (CS) technology for higher output powers, higher efficiency, and higher frequency operation. The DARPA Intra/Interchip Enhanced Cooling (ICECool) program [10], which began in 2012, is developing embedded cooling for thermal management of high-power microelectronic devices.

As phased arrays incorporate higher levels of digitization, the need for highly integrated mixed-signal circuits with both analog and digital functionality has increased as well. Multichip module (MCM) techniques are commonly used in microwave and millimeter-wave RF systems, whereby two or more monolithic microwave integrated circuits (MMICs) are directly mounted on a dielectric substrate and connected by wire bonds. Mixed signal MCMs

incorporate both analog and digital IC chips, but performance for high-speed and wide-bandwidth systems is limited by parasitic effects in the input/output (I/O) connections between the chips. The DARPA Technology for Efficient Agile Mixed Signal Microsystems (TEAM) program and the Scalable Millimeter Wave Architectures for Reconfigurable Transceivers (SMART) program [11] developed critical technologies for highly integrated conformal arrays. The DARPA Compound Semiconductor Materials on Silicon (COSMOS) program [12], which started in 2007 and later became part of the DARPA Diverse Accessible Heterogeneous Integration (DAHI) program [13], is focused on developing transistor-scale heterogeneous integration processes to intimately combine high-power CS devices with high-density silicon CMOS circuits.

The DARPA Arrays at Commercial Timescale (ACT) program [14] began in 2014 with the goal of achieving a digitally interconnected phased array building block, from which larger systems can be formed. The desired building block, composed of a common module and a reconfigurable interface, is scalable and customizable for each application, without requiring a full redesign for each application. The ACT program seeks to enable affordable element-level digital arrays with rapid development cycles and is leveraging the earlier DARPA investments in high-speed mixed-signal technologies described previously [12], [13].

In the European community, significant investments were made in phased array technology by a series of Cooperation in Science and Technology (COST) actions. The COST Action 204, which included participants from Germany, Belgium, The Netherlands, France, Italy, Sweden, the U.K., and the European Space Agency (ESA), developed technology for phased array antennas and their novel applications [15]. The COST Action 284 developed innovative antennas for emerging terrestrial and space-based applications [16].

The Square Kilometer Array (SKA) project, a multinational effort with representation from Australia, Canada, China, India, Italy, New Zealand, South Africa, Sweden, The Netherlands, and the U.K., has been developing innovative phased array technology for radio astronomy applications since 1993 [17].

In the late 1980s, a series of investments were made by the Japanese Ministry of Defense (MOD) to develop conformal airborne phased arrays with element-level digital beamforming [18]. The program developed three large conformal digital beamforming array prototype systems and experimentally demonstrated many of the key benefits of digital arrays. In the same time frame, the FGAN research group in Germany demonstrated a subarray digital beamforming system named Electronically Steerable Radar (ELRA) for investigating digital pattern shaping and adaptive jammer suppression [19].

Simultaneously, the commercial semiconductor industry is progressively improving the state of the art in silicon-based digital processing technology. As shown at the bottom of Fig. 1, the minimum gate lengths, referred to as processing "nodes," have been decreasing in size at a rate predicted by Gordon Moore. Referred to as Moore's Law [20], this decrease in gate length translates directly into higher densities of digital transistors per unit area of integrated circuit chip, and thus enables faster digital processors. These steady improvements in digital processing nodes are driven by commercial market forces.

II. PASSIVE PHASED ARRAYS

The earliest electronically steered phased arrays utilized a centralized high-power transmit amplifier and receiver as shown in Fig. 2. Passive arrays are a natural evolution from large parabolic dish antennas, which also use a centralized transmitter source. The passive array architecture requires the use of low-loss beamformers and phase shifters because the RF losses on the output path from the transmit amplifier to free space translate directly into signal loss and, thus, reduced radar sensitivity. High-power centralized transmitters typically utilize klystron vacuum tube amplifiers or traveling wave tube (TWT) amplifiers, both of which are capable of outputting hundreds of kilowatts of peak power at microwave frequencies. Ferrite phase shifters are commonly used in passive arrays since they are capable of handling very high levels of microwave power with very low insertion loss [21].

Passive phased array architectures are used in a number of significant U.S. military radar systems, including the S-band Aegis phased array radar developed for the U.S. Navy by RCA, the C-band Patriot radar developed for the U.S. Army by Raytheon, and the X-band J-STARS developed for the U.S. Air Force by Grumman [21].

A number of shortfalls are associated with passive arrays. First, the centralized transmit power amplifier is a single point of failure. Second, the low-loss beamformer

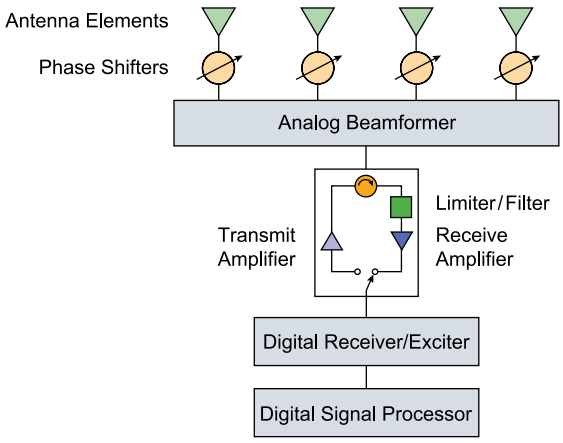

Fig. 2. ***Passive phased array architecture.***

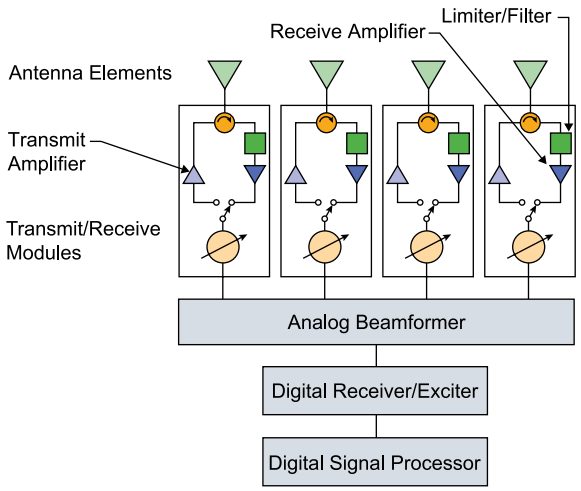

Fig. 3. ***Active phased array architecture.***

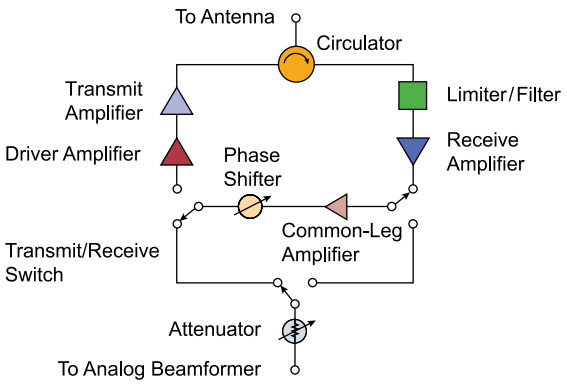

Fig. 4. ***Active phased array T/R module block diagram, with common leg topology.***

networks are large, heavy, and difficult to integrate onto airborne or space-based platforms. Finally, the RF losses incurred in the passive beamformer network and the phase shifters significantly limit radar performance. As noted in Section I, these factors led to a set of sustained investments by DARPA in the late 1980s and 1990s to develop active phased array technology.

III. ACTIVE PHASED ARRAYS

In order to overcome the RF losses imposed by a passive phased array beamformer, the transmit and receive amplifiers can be distributed to each element of the array, as shown in Fig. 3. This approach has the advantage that much lower RF losses are incurred between the transmit amplifiers and free space. This change reduces the noise figure of the array by a factor of two or more, resulting in improved sensitivity and longer operating ranges. A second advantage is that the active phased array architecture "fails" gracefully with the loss of transmit amplifiers at the element level. If the failures are distributed in a random fashion across the array, it is possible to tolerate a loss of 5%–10% of the amplifiers, while maintaining acceptable array performance.

An active array transmit/receive (T/R) module block diagram is shown in Fig. 4. Low-loss RF switches are incorporated into the module to configure the RF path for either high-power transmit or low-noise receive operation.

A circulator, which is a three-port RF device that passes signals in one direction only, is used along with a limiter to protect and isolate the sensitive receive amplifier from the high-power transmit signal. To minimize MMIC area, a common leg topology is often used in T/R module design. The common leg enables the shared use of a phase shifter and gain block for transmit and receive operation. A programmable attenuator is included to provide adjustable amplitude tapers across the array, and to compensate for variations in amplitude as a function of phase shifter state and IC manufacture.

An active X-band T/R module, developed by Raytheon for Missile Defense applications, is shown in Fig. 5 and is representative of high-performance T/R modules used in modern phased arrays. Much of the technology used in these T/R modules was enabled by DARPA MIMIC, HDMP, and MAFET programs described in Section I. Active electronically scanned arrays (AESAs) are now used in a number of U.S. military and commercial systems, including the Theater High Altitude Area Defense (THAAD) ground-based radar, the SPY-3 ship-based radar, the Ground/Air Task-Oriented Radar (G/A-TOR) expeditionary radar, military fighter aircrafts (F-15, F-16, F/A-18, F-22, F-35), and on the Iridium telecommunication satellites [22].

IV. SUBARRAY DIGITAL PHASED ARRAYS

In situations where it is difficult to achieve radar volume search times with a single beam, a subarray digital beamforming architecture has been adopted that provides multiple simultaneous beams over a limited scan sector. As

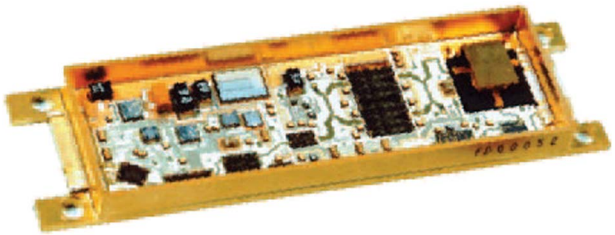

Fig. 5. ***Active X-band T/R module (used with permission from Raytheon).***

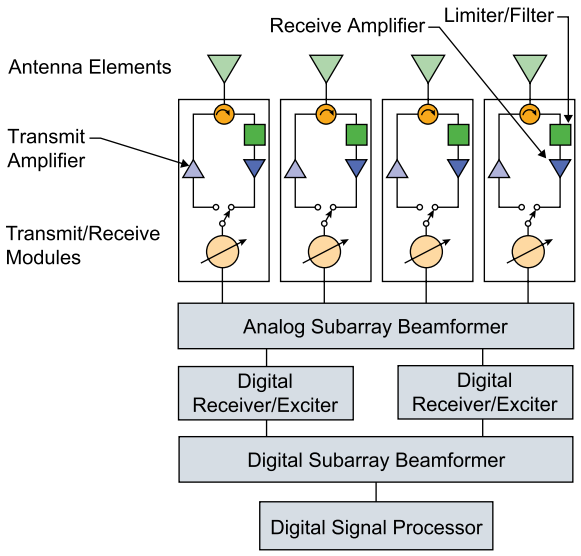

Fig. 6. ***Subarray digital phased array architecture.***

shown in Fig. 6, the subarray digital architecture incorporates a combination of analog and digital beamformers. In this approach, an analog overlapped subarray network produces a flat-topped sector pattern with low sidelobes [23], as shown in Fig. 7. The outputs of each analog subarray are down-converted and digitized. Using a digital processor, the subarray outputs are weighted and summed digitally to produce a set of digital beams within the limited angle of the subarray beam pattern. The low sidelobes of the overlapped subarray pattern suppress the unwanted sum beams, referred to as grating lobes [21], which result from the wide spacing of the digital phase centers.

The overlapped digital subarray architecture represents a compromise between the number of simultaneous beams and the number of digital channels required in the system. Depending on the angle extent of the limited scan sector, the analog overlapped subarray can be complex to build and calibrate [24]. An alternative to a passive overlapped beamformer network is to implement the weighting and summing function using a set of active RF integrated circuit (RFIC) chips, as described in [25]. Contiguous randomly sized digital subarrays can also be used to provide digital beam clusters over a limited angle sector [19], [26], [27]. All of these digital subarray architectures provide adaptive degrees of freedom that can be used to form pattern nulls and implement sophisticated spatial processing techniques.

In cases where cost is a major consideration and multiple simultaneous beams are required over a limited angle sector, the digital subarray architecture provides an attractive solution [28].

V. ELEMENT-LEVEL DIGITAL PHASED ARRAYS

As the cost, size, and power consumption of digital receivers/exciters and processors go down, the use of element-level digital beamforming (DBF) becomes an increasingly realistic approach to implementing large phased arrays. In a DBF array, the received signals are detected and digitized at the element level, and then are processed in a special-purpose digital computer to form the desired beams. On transmit, the output signals for each element are synthesized digitally and then up-converted to RF. A block diagram of a typical element-level DBF architecture is shown in Fig. 8. Each element of the array has a separate digital receiver-exciter (DREX).

There are several key features to the element-level DBF approach. First, the total information available at the aperture is preserved, represented by the N individual element signals, in contrast to an analog beamformer, which produces the weighted sum of these signals and reduces the signal dimensionality from N to 1. A second

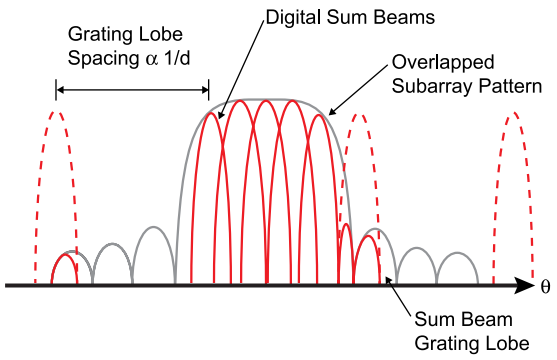

Fig. 7. ***Overlapped subarray digital beam patterns (subarray spacing = d).***

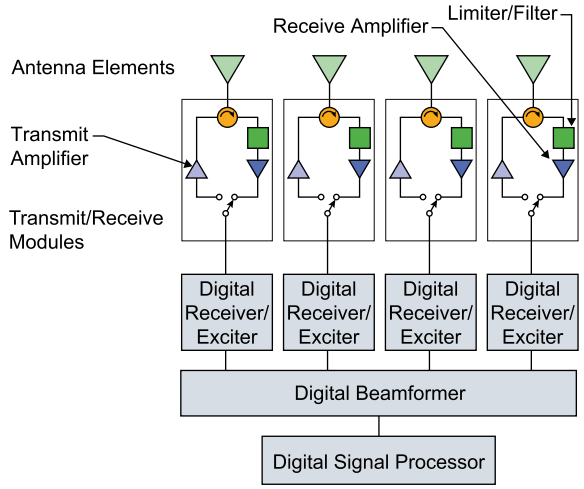

Fig. 8. ***Element-level digital phased array architecture.***

feature is that once the element receive signals have been digitized, they can be manipulated indefinitely because a digital representation of the signal is used rather than the real received signal power. Thus, any number of beams can be formed, and the signal can be subjected to multiple hypothesis testing without degrading signal quality. In DBF, the phase shifting operations of the array are implemented digitally, which allows for arbitrary time delays at each element. This is important for the operation of large arrays over wide bandwidths, where true time delay steering becomes necessary to avoid unwanted beam "squint" effects [23].

The main operational advantages of DBF are as follows: improved adaptive pattern nulling, multiple simultaneous beams over the full scan volume, antenna self-calibration, ultra-low sidelobes, array element pattern correction, and flexible radar power and time management [29].

A key challenge in implementing element-level DBF is the need for an RF transceiver and digitizers at every element of the array. Recent advances in silicon-based RF integrated circuit design and fabrication have paved the way towards low-cost element-level digital transceivers with low power and small form factors [30].

The DARPA ACT program [14] is currently developing highly reconfigurable digital transceiver chips with embedded DBF processing that operate over wide bandwidth with low dc power consumption. Other DARPA programs, such as COSMOS [12], are exploring mixed-signal technologies that will enable further improvements in processing bandwidth, system efficiency, and cost.

For low-power arrays at millimeter-wave frequencies, significant progress has been made in integrating complete phased arrays on RF integrated circuits in SiGe BiCMOS technology [31]. This approach has the potential for extremely low-cost arrays for high-volume commercial applications such as automotive radar.

VI. LOW-COST PHASED ARRAYS

The implementation of a phased array requires a large number of electronic components, including MMICs, multilayer RF printed circuit boards (PCBs), and RF cables and connectors. These components tend to drive the cost of phased arrays and limit their usage to military applications. A typical cost distribution for military radar is shown in Fig. 9, where the phased array represents nearly half of the recurring cost of the system. In the phased array portion of the radar, about half of the cost of the phased array is in the T/R modules. In order to broaden the use of phased arrays, a significant reduction in cost is necessary. Based on the cost distribution in Fig. 9, the best opportunity for cost reduction is in the T/R modules, the RF boards, and the cabling.

Several factors contribute to the high cost of T/R modules. These factors, in order of cost, are the MMICs, the housing, the ceramic substrates, other electrical/

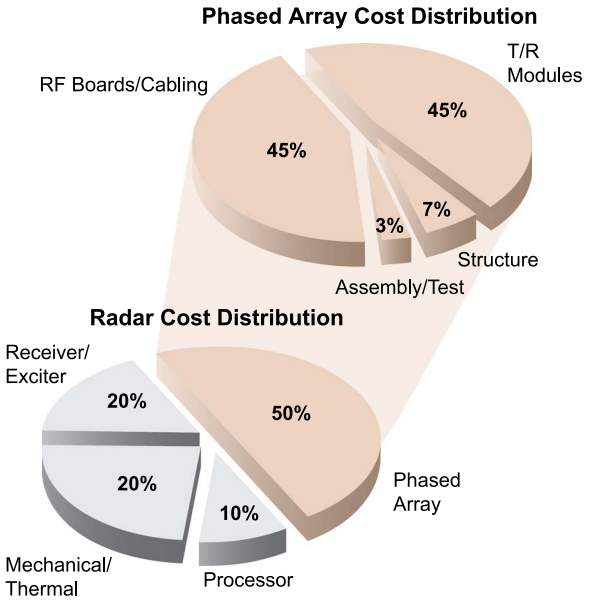

Fig. 9. *Typical cost distribution for phased array radar.*

electronic componentry, and assembly, test, and quality control labor. To first order, MMIC costs are driven by total IC area, the choice of IC technology, and market forces. In some cases, where there has been overlap in commercial and military need for MMICs in terms of frequency or function, the defense marketplace has benefited from much lower MMIC costs. Examples of this benefit are predominantly in the commercial wireless bands at L-, S-, and C-bands.

The T/R module housing provides environmental protection and electrical isolation, and the cost is directly proportional to the sophistication of the design. Traditional module housings are hermetically sealed, gold-plated boxes that incorporate materials with disparate thermal conductivities that must be matched for thermal expansion. Connectors that penetrate the housing walls must also be hermetic. A typical T/R module housing is as shown in Fig. 5. Most housing designs are tailored to the specific application. Factors that drive housing design include the aperture lattice dimensions, heat dissipation of the active components, hermetic sealing method, connectors, and the method of attaching the module to the next-level assembly.

The substrates employed in T/R modules are ceramic-based materials with gold or silver trace metals. Common implementations include thin- and thick-film alumina, and low- and high-temperature co-fired ceramics (LTCC/HTCC). Other electrical components in the module include capacitors, resistors, circulators, power conditioning circuits, and control circuits.

The traditional manufacturing technique used to build T/R modules is called "chip-and-wire." In chip-and-wire assembly, MMICs and other ICs are handled in bare die

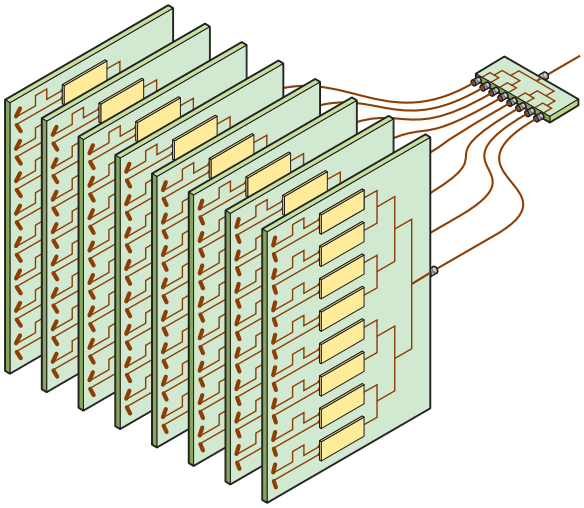

Fig. 10. *Example slat array configuration.*

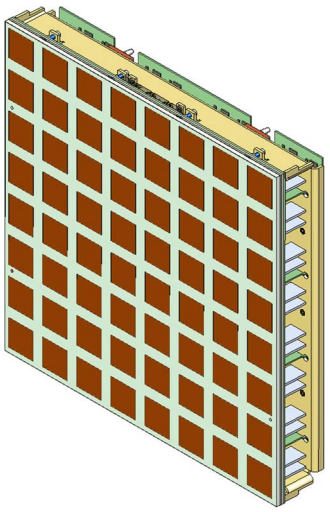

Fig. 11. *Example tile array configuration.*

form, and are done so in a humidity-controlled clean room environment. As opposed to plastic encapsulated MMICs used in commercial manufacture, IC in die form require additional touch labor before use including on-wafer test, visual inspection, and packaging for shipment. As a result, the cost of an IC in die form can be many times more than its commercially packaged equivalent. Die interconnects are made with gold wire or ribbon, and dies are attached with silver epoxy or gold-tin solder. Resistor and capacitor metallurgy must be compatible with these materials, thus increasing the cost of chip-and-wire assemblies. For example, a capacitor for a chip-and-wire assembly would cost \$0.50–\$1.00, whereas a similar one for commercial (solder-based) manufacture would be \$0.001.

Following the T/R modules, traditional phased array cost is driven by the multilayer RF boards and cables. This is made clear by considering the current approach to constructing large phased arrays, depicted in Fig. 10. This architecture is commonly referred to as a slat array, which consists of a series of slats that are oriented perpendicular to the face of the array. The slat approach has the advantage of providing a large surface area for attaching the T/R modules and supporting electronic components. In addition, the high-power amplifier thermal load can be spread out over a large volume—the aperture area times the depth of the slat. A key disadvantage is that it requires a large number of RF boards and cabling to route the RF, dc, and control signals on and off of the slats for array operation.

An alternative approach to building phased arrays is shown in Fig. 11. In this approach, commonly referred to as a tile architecture, the array is constructed of layers that are oriented parallel to the face of the array. The antenna elements and RF beamformers are integrated into a single multilayer RF board, with the T/R modules mounted directly onto the back of the board. This approach has the impact of significantly reducing the area of the RF boards and dramatically reduces the number of connectors and cables. For example, assuming a 5-cm element spacing at S-band, a 1-ft-deep slat array requires 6 m^2 of board area versus 1 m^2 for a tile array.

In the low-cost tile approach, the T/R modules are designed and developed to leverage high-volume commercial microwave packaging and manufacturing techniques. Fig. 12 shows a sample T/R module developed for the Multifunction Phased Array Radar (MPAR) program [29] under support from the Federal Aviation Administration (FAA) and the National Oceanic and Atmospheric Administration (NOAA). The T/R module MMICs are packaged in low-cost commercial packages, referred to as Quad Flat No-lead (QFN). The QFN packages are directly soldered onto an inexpensive PCB, which is then soldered directly to the back of the tile. It should be noted that the QFN packages are nonhermetic, and the environmental control for protection of the components must be accomplished at the tile or array level, rather than at the T/R module level. The RF and dc interconnections between the T/R module and the back of the tile consist of simple metal pads that line the edges of the printed circuit board, as shown in Fig. 12. The MPAR T/R module also uses transmit-receive switches instead of circulators, which further reduces cost and size. Low-loss T/R switches are implemented using PIN diodes, with insertion loss comparable to a circulator. Because of the compactness of the design, RF signal transmission line length in the T/R module substrate is < 2 cm. As a result, low-cost, high-loss tangent (> 0.01) substrates can be employed instead of high-cost, low-loss tangent (< 0.004) materials. The net penalty in added insertion loss of the transmission line is

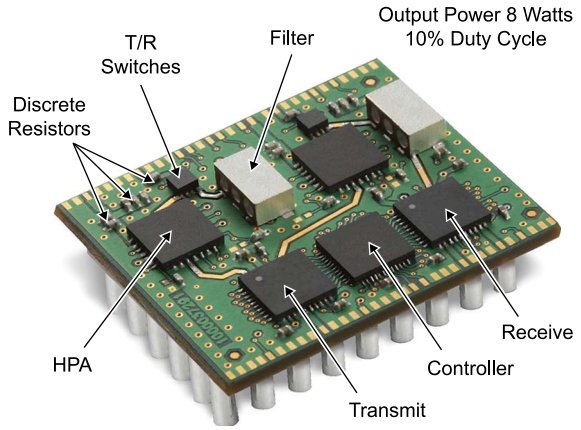

Fig. 12. ***Low-cost MPAR T/R module.***

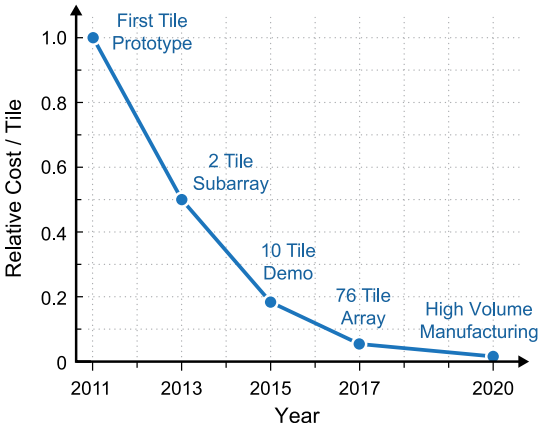

Fig. 14. ***Relative cost per 64-element MPAR tile over time.***

< 0.1 dB. In high volume, the cost of the MPAR T/R module is projected to be ~$25 with the bulk of that number going to the MMIC cost. The cost of the substrate, componentry, assembly, and test is < $5.

Fig. 13 shows a fully assembled MPAR tile, which provides a low-cost, scalable building block for large array apertures. As the volume of manufacturing increases, investments in automated assembly and test equipment bring down the cost per unit and improve yield of the MPAR tiles. Fig. 14 shows the relative cost of the MPAR tiles as a function of time and clearly indicates the significant cost benefits made possible by the approach.

A simple cost model described in the Appendix can be used to understand the differences between the slat and tile architectures. A key difference between the slat and tile array architectures is the area of the RF boards. Many of the costs are proportional to the number of RF boards and the total board area. The number of slats per unit area of array increases directly with frequency because slats are typically spaced at one-half wavelength intervals. As a result, the cost differences between the slat and the tile arrays will be larger at higher frequencies.

An example of the cost per unit area for a slat array and a tile array is shown in Fig. 15. The parameters and assumptions used to calculate these individual costs are given in the Appendix. This example assumes identical RF chip set cost. The higher cost of the slat array is due to the metal T/R module packages, the increased RF board area, and the cooling apparatus (which is proportional to RF board area).

Using the cost model in the Appendix, the relative transmit power per unit area versus cost per unit area for

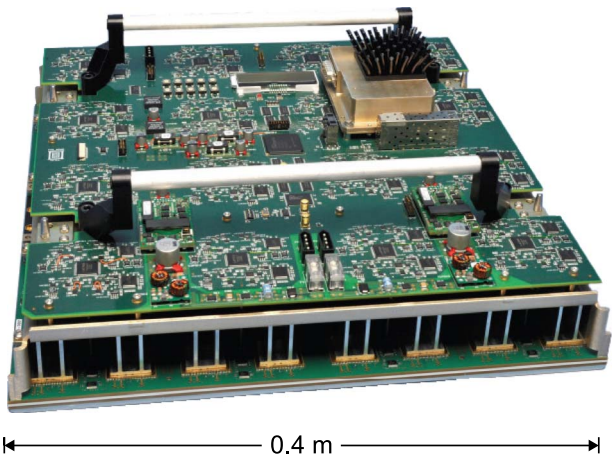

Fig. 13. ***Fully assembled MPAR tile.***

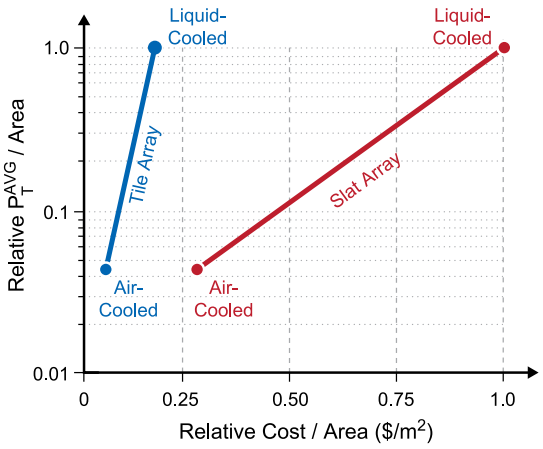

Fig. 15. ***Relative transmit power per unit area versus cost per unit area for tile and slat arrays.***

Table 1 Example Cost Comparison for Slat Versus Tile

Component	Slat ($/m^2)	Tile ($/m^2)
T/R Chip Set	$80,000	$80,000
Die Handling	$40,000	N/A
T/R Module Packages	$400,000	$8,000
RF Boards	$150,000	$25,000
Cables & Connectors	$10,000	$1,562
Cooling	$180,000	$40,000
Structure	$50,000	$16,250
Assembly & Test	$80,000	$12,500
Total	$990,000/m^2	$183,312/m^2

both the slat and tile arrays is plotted in Fig. 15 for two different transmit power levels. This example shows an improvement ratio of more than 5:1 in cost per unit area for both the low-power and high-power cases. For both cases, the dominant cost drivers for the slat array are the RF board area and the T/R module packaging. By minimizing the RF board area, utilizing low-cost T/R packaging, and leveraging high-volume manufacturing and test techniques, the tile array architecture provides a low-cost alternative to slat arrays, as shown in Table 1.

A critical challenge for tile arrays at high-power densities is the integration of a coldplate into the thin tile structure. In order to maintain low cost at higher power levels, a thin two-dimensional heat exchanger must be incorporated into the PCB stackup using standard high-volume manufacturing techniques. This is a technology that is currently being investigated.

VII. FUTURE DIRECTIONS

One of the major cost drivers for both the slat and the tile arrays at higher power densities is the cost of the transmit power amplifiers. Currently, the phased array industry is utilizing state-of-the-art GaN-on-SiC MMIC technology, due to the high operating efficiency and smaller die areas of GaN. However, the cost of GaN-on-SiC is relatively high, due to the use of specialized, low-volume fabrication facilities and the high cost of SiC wafers. Recent work has shown that GaN can be grown directly onto low-cost Si wafers and processed in standard commercial Si foundries [32]. This approach has the potential to reduce the cost per watt for GaN power amplifiers by a factor of 10×. It also opens up the possibility for integrating Si CMOS circuits with high power GaN circuits by 3-D bonding of GaN-on-Si wafers with Si CMOS wafers [33]. This would enable a powerful combination of RF and digital technologies to be integrated onto a single chip at a very low cost and would have a significant impact on the future cost of high-power phased arrays. A high-power, mixed-signal circuit capability on a single chip would also improve the possibility of building highly capable element-level digital arrays with relevant output power levels at low cost. New array functionalities, such as simultaneous transmit and receive (STAR), will require sophisticated RF and digital cancellation techniques at the element or subarray level and are a potential future application of a high-power mixed-signal technology available at a reasonable cost.

VIII. CONCLUSION

Electronically scanned phased arrays provide significant performance benefits over mechanically scanned antennas. High levels of maturity in solid-state microwave integrated circuits have enabled the widespread use of phased arrays in military systems, but the cost remains high. The use of high-volume commercial microwave manufacturing techniques has the potential to dramatically lower the cost of phased arrays. Furthermore, the rapid evolution of digital processor technology is fostering the emergence of fully digital arrays, with significant improvements in performance. Future arrays will leverage current investments in high-speed mixed-signal integrated circuits to operate over wide signal bandwidths and perform multiple simultaneous functions. ■

APPENDIX

A simple cost model can be used to understand the differences between the slat and tile architectures. For both array types, the cost of a phased array can be expressed as

$$\begin{aligned}\text{Cost}_{\text{Array}} &= \text{Cost}_{\text{T/R Module}} + \text{Cost}_{\text{RF Boards}} \\ &\quad + \text{Cost}_{\text{Cables/Connectors}} + \text{Cost}_{\text{Cooling}} \\ &\quad + \text{Cost}_{\text{Structure}} + \text{Cost}_{\text{Rf Assembly/Test}} \end{aligned} \tag{1}$$

where

$$\begin{aligned}&\text{Cost}_{\text{T/R Modules}} \\ &\quad = (\text{Cost}_{\text{RF Chip Set}} + \text{Cost}_{\text{Die Handling}} \\ &\qquad + \text{Cost}_{\text{T/R Package}}) \times N_{\text{Elements}}\end{aligned} \tag{2}$$

$$\begin{aligned}&\text{Cost}_{\text{RF Boards}} \\ &\quad = \text{Cost per m}^2\text{ RF board} \times \text{Area}_{\text{RF Boards}}\end{aligned} \tag{3}$$

$$\begin{aligned}&\text{Cost}_{\text{Cables/Connectors}} \\ &\quad = \text{Cables/Connectors cost per RF Board} \\ &\qquad \times N_{\text{RF Boards}}\end{aligned} \tag{4}$$

$$\begin{aligned}&\text{Cost}_{\text{Cooling}} \\ &\quad = \text{Cooling cost per m}^2\text{ RF Board} \times \text{Area}_{\text{RF Boards}}\end{aligned} \tag{5}$$

$$\text{Cost}_{\text{Structure}} = \text{Structure cost per m}^2_{\text{Array}} \times \text{Area}_{\text{Array}} + \text{Structure cost per RF Board} \times N_{\text{RF Boards}} \quad (6)$$

$$\text{Cost}_{\text{RF Assembly/Test}} = \text{Assembly/Test cost per RF Board} \times N_{\text{RF Boards}} \quad (7)$$

For Slat Arrays :

$$\text{Area}_{\text{RF Boards}} = \text{Area}_{\text{Slat}} \times N_{\text{RF Boards}} \quad (8)$$

For Tile Arrays :

$$\text{Area}_{\text{RF Boards}} = \text{Area}_{\text{Array}}. \quad (9)$$

As an example, the model was used to compute the cost of slat and tile arrays at 3.0 GHz (S-band) for two different transmit power levels. In this example, the following assumptions were made:

Slat Array :

$$\text{Cost}_{\text{RF Chip Set}} = \$25.00 \text{ (Low Power)}, \$200.00 \text{ (High Power)} \quad (10)$$

$$\text{Cost}_{\text{Die Handling}} = \$75.00 \text{ (Low Power)}, \$100.00 \text{ (High Power)} \quad (11)$$

$$\text{Cost}_{\text{T/R Package}} = \$600.00 \text{ (Low Power)}, \$1000.00 \text{ (High Power)} \quad (12)$$

$$\text{Cost per m}^2 \text{ RF Board} = \$25,000.00 \quad (13)$$

$$N_{\text{RF Boards}} = 40 \text{ per m}^2 \text{ array} \quad (14)$$

$$\text{Area}_{\text{Slat}} = 0.15 \text{ m}^2 \quad (15)$$

$$\text{Cables/Connectors cost per RF Board} = \$250.00 \quad (16)$$

$$\text{Cooling cost per m}^2 \text{ RF Board} = \$10,000.00 \text{ (Low Power)}, \$30,000.00 \text{ (High Power)} \quad (17)$$

$$\text{Structure cost per m}^2_{\text{Array}} = \$10,000.00 \quad (18)$$

$$\text{Structure cost per RF Board} = \$1,000.00 \quad (19)$$

$$\text{Assembly/Test cost per RF Board} = \$2,000.00 \quad (20)$$

Tile Array :

$$\text{Cost}_{\text{RF Chip Set}} = \$25.00 \text{ (Low Power)}, \$200.00 \text{ (High Power)} \quad (21)$$

$$\text{Cost}_{\text{Die Handling}} = \text{N/A} \quad (22)$$

$$\text{Cost}_{\text{T/R Package}} = \$5.00 \text{ (Low Power)}, \$20.00 \text{ (High Power)} \quad (23)$$

$$\text{Cost per m}^2 \text{ RF Board} = \$25,000.00 \quad (24)$$

$$N_{\text{RF Boards}} = 6.25 \text{ per m}^2 \text{ aperture} \quad (25)$$

$$\text{Cables/Connectors cost per RF Board} = \$250.00 \quad (26)$$

$$\text{Cooling cost per m}^2 \text{ RF Board} = \$10,000.00 \text{ (Low Power)}, \$40,000.00 \text{ (High Power)} \quad (27)$$

$$\text{Structure cost per m}^2_{\text{Array}} = \$10,000.00 \quad (28)$$

$$\text{Structure cost per RF Board} = \$1,000.00 \quad (29)$$

$$\text{Assembly/Test cost per RF Board} = \$2,000.00. \quad (30)$$

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