For $i_a = 0$ this implies that

$$\frac{dw_r}{dt} = -Dw_r$$

$$\frac{di_f}{dt} = -Hi_f + Iv.$$

For $i_f = 0$ this implies that

$$\frac{di_a}{dt} = -Ai_a + Cv$$

$$\frac{dw_r}{dt} = -Dw_r$$

either of which is stable.

Conclusion 6: The shunt-connected motor is input-output with output linearizable with $y = T_e$, provided $Ci_f + Ii_a \neq 0$.

V. Conclusions

The feedback linearization of series- and shunt-connected motors has been studied. It has been found that they can be feedback linearized in a variety of ways. The series-connected motor can input-to-state linearized, whereas the shunt-connected motor cannot. All of the feedback linearizations are valid except on "thin sets" of states.

References

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Techniques for Improving Resolver-to-Digital Conversion Accuracy

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Abstract—**Tracking resolver-to-digital converters are often used with resolvers to form a high-accuracy position sensor. When resolver signals deviate from the assumed ideal, the converter output exhibits error, degrading position accuracy. In this letter, resolver signal-processing techniques are introduced that reduce or eliminate the position error incurred due to common resolver signal imperfections. In particular, a method is introduced that eliminates the error due to imperfect quadrature. In addition, several techniques are discussed that reduce the position error caused by resolver inductance harmonics.**

I. Introduction

Manufacturers of tracking resolver-to-digital (R/D) converters state position resolution and accuracy specifications under the assumption that ideal resolver signals are supplied to the converter. In reality, no resolver generates ideal signals and thus the accuracy specifications of an R/D converter can never be met in practice. In prior work by the author [1], the effects of common resolver signal imperfections on position accuracy were presented. In this letter, resolver signal processing techniques are discussed that reduce or eliminate the position error incurred due to these imperfect characteristics. In particular, a method is introduced that eliminates the error due to imperfect quadrature. In addition, several techniques are discussed that reduce the position error caused by resolver inductance harmonics. The letter proceeds as follows: first, ideal R/D conversion is reviewed to introduce basic concepts and terminology. Second, the position error incurred due to common imperfect resolver signal characteristics are summarized. Finally, signal-processing techniques to reduce or eliminate position error are discussed.

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II. Resolver-to-Digital Conversion

A. Ideal R/D Conversion

The signals generated by an ideal resolver can be written as [1]

$$V_s = V_1 \sin\theta \cos\omega t$$

$$V_c = V_1 \cos\theta \cos\omega t$$

where V_1 is a constant that depends on the construction of the resolver and the resolver excitation level, θ is the position to be decoded, and $\cos\omega t$ is the excitation signal. Given the operational block diagram of a tracking R/D converter as shown in Fig. 1, the operation of an ideal R/D converter is described as follows [1], [2]. First the inputs to the R/D converter (1) are multiplied by $\cos\phi$ and $\sin\phi$, respectively, where ϕ is the converter's current estimate of the actual position θ. Second, the difference between the two signals is found, giving the error voltage,

$$\begin{aligned} V_{\text{err}} &= V_1 \sin\theta \cos\phi \cos\omega t - V_1 \cos\theta \sin\phi \cos\omega t \\ &= V_1 \sin(\theta - \phi) \cos\omega t. \end{aligned} \tag{2}$$

This double-sidedband-modulated signal is synchronously demodulated, using the resolver excitation signal as a demodulation reference, leaving the envelope signal

$$E = V_1 \sin(\theta - \phi). \tag{3}$$

Finally, this signal is driven to zero by a type II servo loop with ϕ being the control variable [1]. When this is done, the converter's position estimate ϕ is forced to equal the actual shaft position θ resulting in zero position error. In an actual R/D converter, ϕ is continuously updated and output in digital format.

B. Position Error Sources and Error Expressions

In prior work by the author [1], expressions for the position error incurred due to common resolver signal imperfections were developed. Of the error sources discussed, amplitude imbalance, imperfect quadrature, and inductance harmonics are pertinent to this work and are summarized as follows.

Amplitude imbalance refers to the occurrence of an amplitude difference between the two resolver signals (1). In this case, the resolver signals can be written as

$$\begin{aligned} V_s &= V_1 \sin\theta \cos\omega t \\ V_c &= (1+\alpha) V_1 \cos\theta \cos\omega t \end{aligned} \tag{4}$$

where α represents the amount of amplitude imbalance. Processing these signals by an R/D converter leads to the following expression for the position error ($\epsilon = \theta - \phi$) as a function of position θ

$$\epsilon \approx \frac{\alpha}{2} \sin(2\theta). \tag{5}$$

This error expression is an approximation that is accurate as long as α is small, i.e., less than approximately 5%.

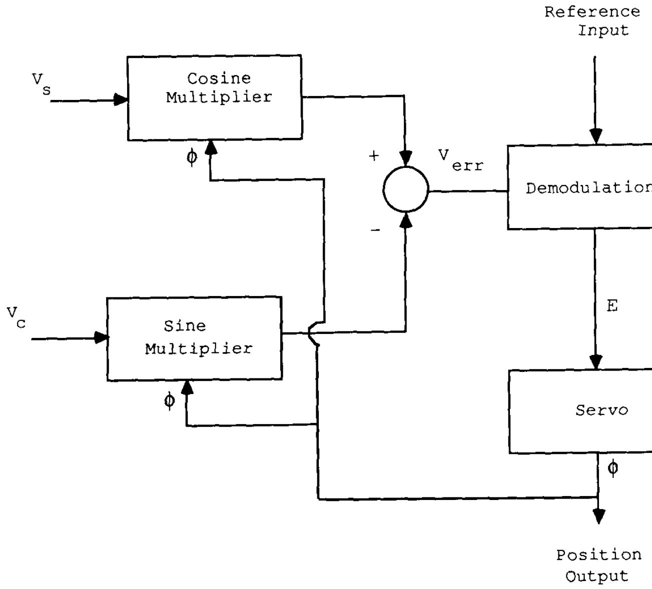

Fig. 1. Resolver-to-digital converter block diagram.

Imperfect quadrature refers to a spatial misalignment between the two resolver phases, that is, the case when the inductance profiles of the two phases are not exactly $\pi/2$ rad out of phase with one another. In this situation, the resolver signals can be written as

$$V_s = V_1 \sin\theta \cos\omega t$$
$$V_c = V_1 \cos(\theta + \beta) \cos\omega t \tag{6}$$

where β is the amount of quadrature error. Application of (6) to an R/D converter leads to an approximate position error in the R/D output of

$$\epsilon \approx \frac{\beta}{2}(1 - \cos 2\theta). \tag{7}$$

Once again this expression is accurate for small β.

In general, it is impossible to construct a resolver with inductance profiles that are perfect sinusoidal and cosinusoidal functions of position. More generally, the inductances will contain harmonics that create resolver output signals of the form

$$V_s = V_1\left\{K_0 + \sum_{n=1}^{\infty} K_n \sin(n\theta)\right\}\cos\omega t$$
$$V_c = V_1\left\{K_0 + \sum_{n=1}^{\infty} K_n \cos(n\theta)\right\}\cos\omega t \tag{8}$$

where K_n is the ratio of the nth inductance harmonic to the fundamental. K_0 is the ratio of the inductive dc component to the fundamental. Application of these signals to an R/D converter leads to a position error of

$$\epsilon \approx -\sqrt{2}\,K_0 \cos(\theta + \pi/4) - \sum_{n=1}^{\infty} K_n \sin((n-1)\theta). \tag{9}$$

Equations (5), (7), and (9) describe how sensitive the R/D conversion process is to these imperfect characteristics. By defining an error bound, it is possible to illustrate this sensitivity. Because the output of an R/D converter is in digital format, it is convenient to define an error bound in terms of a $\frac{1}{2}$ least significant bit (LSB) degradation in position accuracy. Table I gives the magnitude of each imperfect characteristic that degrades the position accuracy by $\frac{1}{2}$ LSB out of 10 and 16 b, respectively.

TABLE I
SUMMARY OF ERROR MAGNITUDES FOR MAXIMUM $\frac{1}{2}$ LSB POSITION ERROR

Position Error Source	Error Bound for $\frac{1}{2}$ LSB Accuracy Degradation Out of: 10 b	16 b
Amplitude imbalance	0.62%	0.0096%
Imperfect quadrature	3.1E-3 rad	4.8E-5 rad
DC inductive component	0.22%	0.0034%
Single harmonic	0.31%	0.0048%

It is clear from the table that the R/D conversion process is very sensitive to resolver signal imperfections. For example, an amplitude imbalance of 0.62% is all that is required to create a $\frac{1}{2}$-LSB position error out of 10-b resolution. The position error due to inductive harmonics is depicted in the last two rows of the table. The next-to-last row considers the case when only the K_0 term in (9) is present, and the last row assumes the presence of only one term K_n in the summation in (9). For each of these, the figure given in the table is relative to the amplitude of the desired fundamental component of the resolver signal.

III. Position Error Minimization

Of the position error sources listed, amplitude imbalance is the easiest to eliminate. This source of error is eliminated by simply attenuating the larger of the two signals. The remaining two error sources—imperfect quadrature and inductance harmonics—are much more difficult to compensate for. Imperfect quadrature occurs when the two phases in the resolver are not machined or assembled exactly $\pi/2$ rad out of phase with each other. Because this error source affects the position information portion of the resolver signals (6), there is no straightforward way to eliminate the resulting position error. Inductance harmonics present a similar difficulty. The existence of harmonics creates extra position information carrying terms in the resolver signals that are not readily removed. In this section, several methods for reducing or eliminating these more difficult error sources are introduced.

A. Calibration and Correction

Perhaps the easiest way to reduce or eliminate position error due to any and all sources is through calibration against a higher accuracy sensor. In other words, once the position error versus position is measured and known, the actual position can be found by subtracting the error from the R/D converter output. This is readily accomplished by using a PROM to map the incorrect position into the correct position. In this method, the R/D converter output is used as the address for the PROM, with the data stored at each address being the corrected position.

Although the above method is easy to implement, it does require a significant amount of effort as it requires measuring the resolver output at all 2^n output positions. Moreover, depending on the actual error profile, it is probable that the corrected position output will not increment consecutively but will jump over some quantized positions.

An alternative to this method was reported by Hung and Hung [3]. In their work, the error versus position is measured at relatively few points. Using these data, the error versus position is approximated by a Fourier series from which the corrected position for a given reported position is computed in real time by a digital processor.

B. Imperfect Quadrature Error Elimination

The position error due to imperfect quadrature can be eliminated by appropriate processing of the resolver signals prior to conversion by an R/D converter. To illustrate this method, the resolver signals with quadrature error (6) are rewritten here as

$$V_s = V_1 \sin\theta \cos\omega t$$
$$V_c = V_1 \cos(\theta + \beta)\cos\omega t. \qquad (10)$$

Two new signals for R/D conversion are generated by alternately adding and subtracting these two signals. That is, new signals are formed as

$$\hat{V}_s = V_s + V_c$$
$$\hat{V}_c = V_s - V_c. \qquad (11)$$

Substituting (10) into (11) and simplifying, one obtains the new signals to be decoded:

$$\hat{V}_s = [2V_1 \cos\sigma]\sin(\theta + \sigma)\cos\omega t$$
$$\hat{V}_c = [-2V_1 \sin\sigma]\cos(\theta + \sigma)\cos\omega t \qquad (12)$$

where $\sigma = \beta/2 + \pi/4$.

Comparing (12) with the ideal resolver signals (1) shows that quadrature error has been eliminated at the expense of added amplitude imbalance, a sign change, and an offset in decoded angle from θ to $\theta + \sigma$. The term in brackets in (12) causes the amplitude and sign of the two signals to be different, and the fact that $\theta + \sigma$ appears as the argument of the sine and cosine, rather than just θ, implies that the R/D converter will output $\theta + \sigma$. Fortunately, these undesirable side effects are easily corrected. The sign change and amplitude imbalance are easily eliminated by the addition of an inverting gain stage in one of the resolver signal paths. Because σ is a fixed angle, and because the output of the R/D converter is in digital format, it is straightforward to subtract σ from $\theta + \sigma$ using appropriate logic gates or a microprocessor. The only potential difficulty in implementing this technique is in determining σ so that the required subtraction can be accomplished.

C. Inductance Harmonic Cancellation

In an ideal resolver, the inductance profile of each phase is a perfect sinusoid. This ideal can never be achieved in practice because of manufacturing tolerance and because the ideal "sinusoidal winding distribution" [4] can only be approximated. Thus, all resolver signals contain some residual inductive harmonics that can severely decrease the position accuracy of an R/D converter [1].

There is one technique of resolver construction that ideally eliminates all even harmonics in the resolver output signals. This technique requires that two additional phases be added to the resolver, with these phases constructed π rad out of phase with the original two. The voltage induced in these phases are

$$\overline{V}_s = V_1\left[K_0 + \sum_{n=1}^{\infty} K_n \sin(n(\theta - \pi))\right]\cos\omega t$$
$$\overline{V}_c = V_1\left[K_0 + \sum_{n=1}^{\infty} k_n \cos(n(\theta - \pi))\right]\cos\omega t. \qquad (13)$$

Subtracting these signals from their corresponding complementary signals in (8) gives two new resolver signals

$$\hat{V}_s = V_s - \overline{V}_s = 2V_1\left(\sum_{\substack{n=1 \\ n \text{ odd}}}^{\infty} K_n \sin(n\theta)\right)\cos\omega t$$
$$\hat{V}_c = V_c - \overline{V}_c = 2V_1\left(\sum_{\substack{n=1 \\ n \text{ odd}}}^{\infty} K_n \cos(n\theta)\right)\cos\omega t. \qquad (14)$$

Comparing these resolver signals to those in (8) shows that all even harmonics, including the dc component, have been eliminated. In practice, this cancellation is not exact but nevertheless is substantial. In addition, the subtraction performed in (14) is usually accomplished within the resolver itself by the way that it is wound. Applying these signals to an R/D converter changes the position error expression (9) to

$$\epsilon \approx -\sum_{\substack{n=2 \\ n \text{ even}}}^{\infty} K_{n+1}\sin(n\theta). \qquad (15)$$

Thus, the position error expression contains only even harmonics when the resolver signals contain only odd harmonics. Comparing (15) to (9), it is likely, although not guaranteed, that the maximum position error will be less as a result of the elimination of all odd error harmonics.

D. Inductance Harmonic Error Reduction

Comparing (5) and (9) shows that both amplitude imbalance and inductive harmonics produce position error that is sinusoidal with respect to position. This fact implies that it may be possible to use amplitude imbalance to reduce the position error due to inductive harmonics by considering both error sources simultaneously. It is possible to show that this is indeed true. The resolver output signals in the presence of both amplitude imbalance and inductive harmonics can be written as

$$V_s = V_1\left(K_0 + \sum_{n=1}^{\infty} K_n \sin(n\theta)\right)\cos\omega t$$
$$V_c = (1 + \alpha)V_1\left(K_0 + \sum_{n=1}^{\infty} K_n \cos(n\theta)\right)\cos\omega t \qquad (16)$$

where the various terms are defined as they were previously. Application of these signals to an R/D converter produces a position error of

$$\epsilon \approx K_0\left(\alpha \sin\theta + \sqrt{2}\sin\left(\theta - \frac{\pi}{4}\right)\right) - \sum_{n=1}^{\infty} K_n\left\{\left(1+\frac{\alpha}{2}\right)\sin\left[(n-1)\theta\right] - \frac{\alpha}{2}\sin\left[(n+1)\theta\right]\right\}. \quad (17)$$

Rearrangement of the summation in (17) leads to the final result

$$\epsilon \approx \sqrt{2}K_0 \sin\left(\theta - \frac{\pi}{4}\right) + \left[\alpha K_0 - \left(1+\frac{\alpha}{2}\right)K_2\right]\sin(\theta) + \sum_{n=2}^{\infty}\left[\frac{\alpha}{2}K_{n-1} - \left(1+\frac{\alpha}{2}\right)K_{n+1}\right]\sin(n\theta). \quad (18)$$

Inspection of this equation shows that under certain conditions it is possible to reduce the position error due to inductive harmonics by adjusting the amplitude imbalance between the two resolver signals. In particular, if inductive harmonic cancellation is implemented as described in Section III.C, the first two terms in (18) disappear, leaving

$$\epsilon \approx \sum_{\substack{n=2 \\ n\ \text{even}}}^{\infty}\left[\frac{\alpha}{2}K_{n-1} - \left(1+\frac{\alpha}{2}\right)K_{n+1}\right]\sin(n\theta). \quad (19)$$

The term in brackets in (19) is zero when α is chosen as

$$\alpha = \frac{2K_{n+1}}{K_{n-1} - K_{n+1}}. \quad (20)$$

Clearly, it is impossible to choose one α such that (20) holds for all harmonics. However, because it is usually the lowest order ($n = 2$) error harmonic that dominates the position error, α can be chosen to eliminate it. This choice of α will modify the remaining error harmonics, decreasing the amplitude of some and increasing others. Alternatively, because the peak position error is usually of greatest concern, α can be experimentally adjusted so that the peak error is minimized.

IV. Conclusions

In this letter, several methods for reducing the position error caused by the existence of imperfect resolver signal characteristics have been introduced. The most straightforward method is to simply calibrate each resolver and R/D converter, then correct the R/D converter output in real time. Although this method corrects all errors, including those with an origin in the R/D converter, it is also the most time consuming and labor intensive. By appropriate signal processing, it is shown that quadrature error can be eliminated by simple algebraic manipulation of the resolver signals. Similarly, it is shown that all even harmonics in the resolver signals can be canceled if the resolver is constructed with complementary phases. Finally, it is shown that amplitude imbalance can be used to reduce the position error due to inductive harmonics.

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